



### European Conference on Parallel Computing

#### Topic 18: Embedded Parallel Systems

##### Description

Multi-processor systems implemented in System-on-a-Chip technology (MPSoC) are emerging for processing embedded applications such as consumer electronics, mobile phones, computer graphics, and medical imaging, to name a few. Contrary to cluster and grid processing, their design and required compilation techniques are driven by multiple conflicting design objectives simultaneously such as power consumption, speed, monetary cost, and physical as well as memory size. Here, new specification techniques, special parallelization and mapping techniques are needed in order to embed computations optimally into the parallel architecture. Particularly welcome are also new and emerging architecture concepts ranging from fine-grain to coarse-grain parallel SoC architectures with focus on dynamic programmability or reconfigurability. Finally, case studies of embedded, highly-parallel applications are greatly welcome.

##### Focus

- System-on-a-Chip Multi-core/Multithreaded Architecture Design
- Low Power Compilation and Architecture Design
- Interconnection Structures of Processors and Memory Modules
- Reconfigurability versus Programmability
- Multi-processor based Reconfigurable Architectures
- Processors with tightly coupled Reconfigurable Hardware
- Modeling and Simulation Techniques for MPSoC
- Memory/Performance/Cost Analysis , Estimation
- Architecture/Compiler Co-Design
- Embedded, Highly-Parallel Applications
- Parallelization and Mapping Techniques for MPSoC

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